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| --- | --- |
| Name: Adan Shahid | EE-272L Digital Systems Design |
| Reg. No.: 2022-EE-119 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

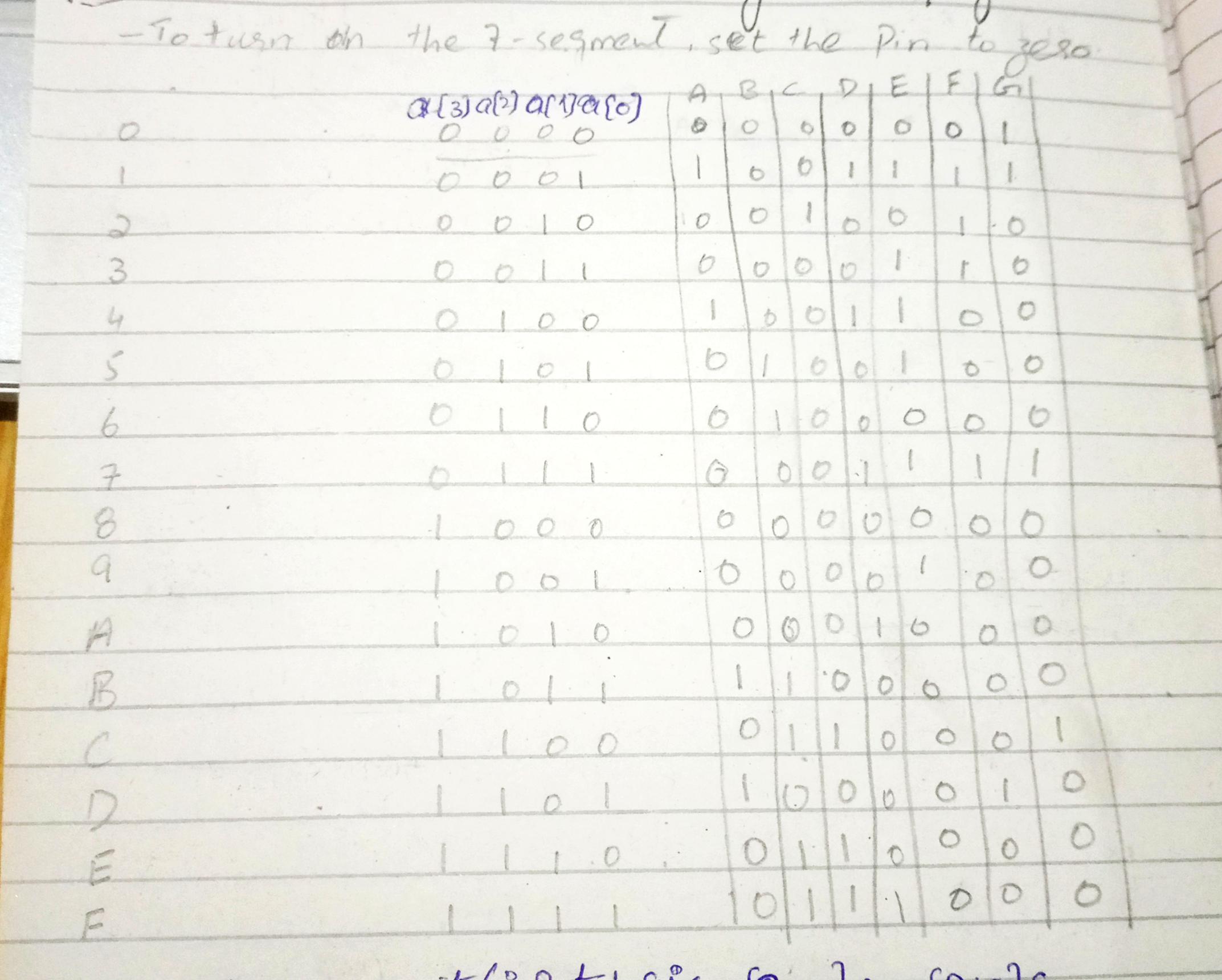


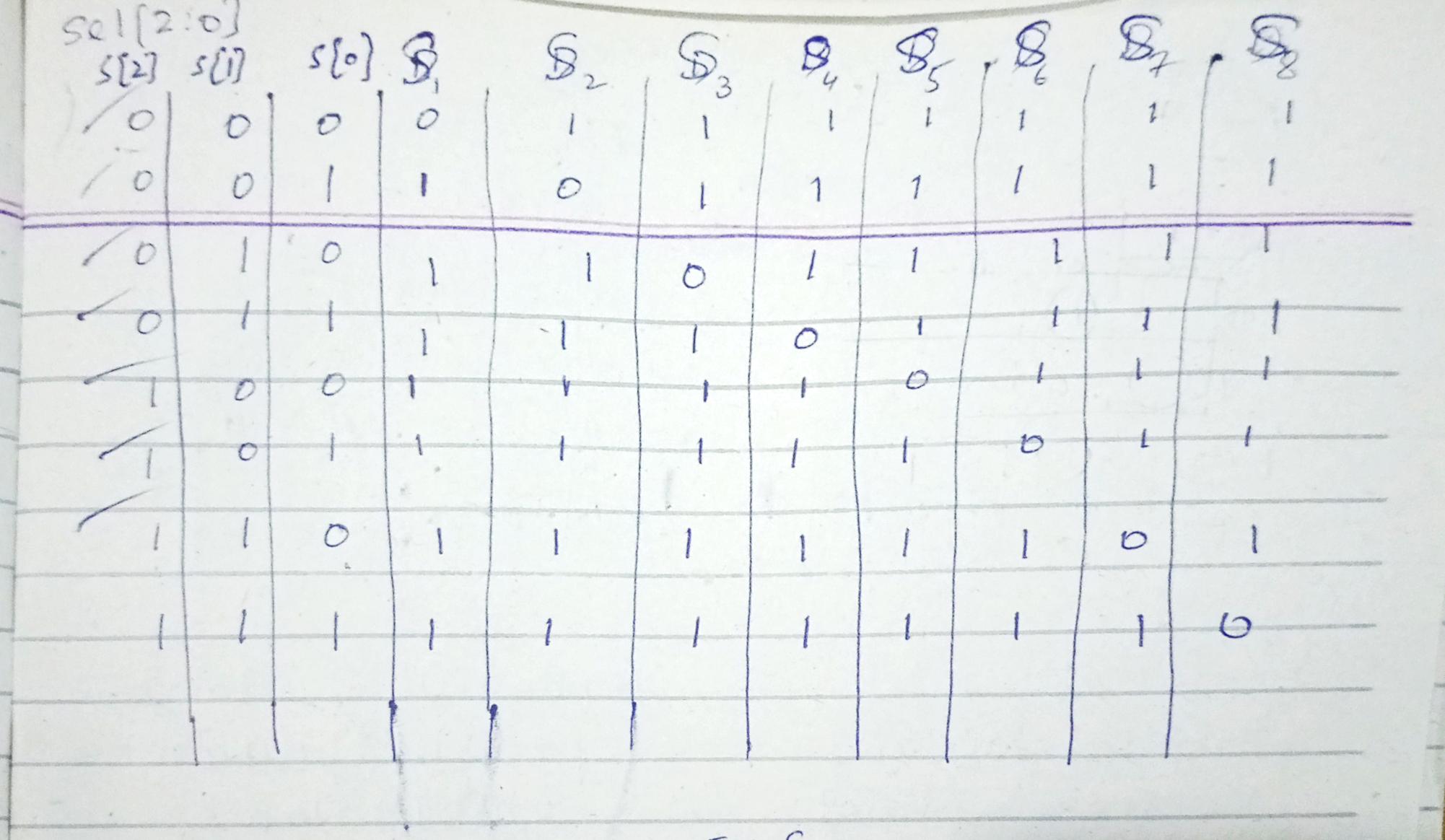
**Lab Manual**

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| --- | --- | --- | --- | --- | --- |
| **DSD Lab Manual Evaluation Rubrics** | | | | | |
|  |  |  |  |  |  |
| **Assessment** | **Total Marks** | **Marks Obtained** | **0-30%** | **30-60%** | **70-100%** |
| Code Organization | 3 |  | No Proper Indentation and descriptive naming, no code organization.  Zero to Some understanding but not working | Proper Indentation or descriptive naming or code organization.  Mild to Complete understanding but not working | Proper Indentation and descriptive naming, code organization.  Complete understanding, and proper working |
| Simulation | 5 |  | Simulation not done or incorrect, without any understanding of waveforms | Working simulation with errors, don't cares's(x) and high impedance(z), partial understanding of waveforms | Working simulation without any errors, etc and complete understanding of waveforms |
| FPGA | 2 |  | Not implemented on FPGA and questions related to synthesis and implementation not answered. | Correctly Implemented on FPGA or questions related to synthesis and implementation answered. | Correctly Implemented on FPGA and questions related to synthesis and implementation answered. |

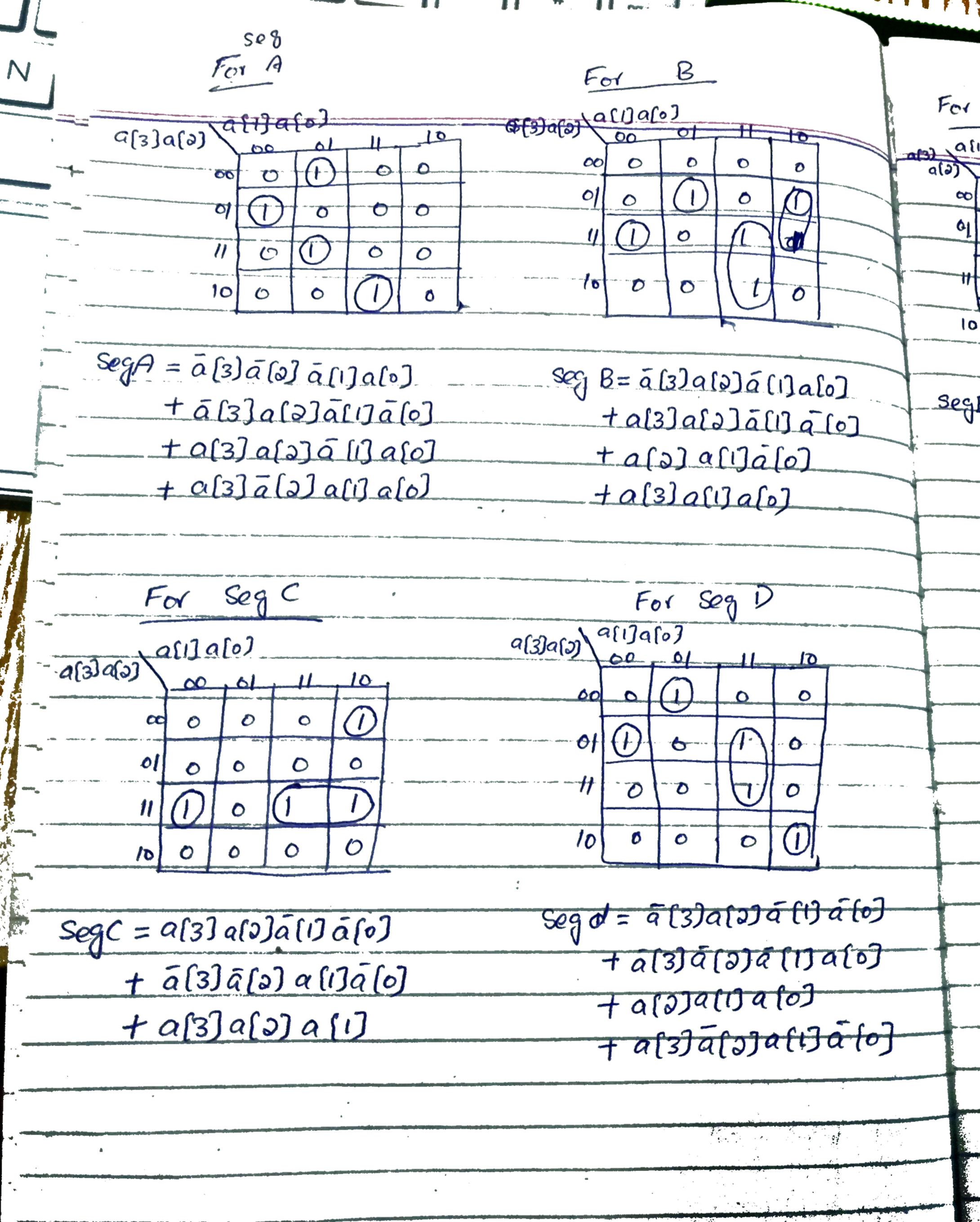
**Part (1)**

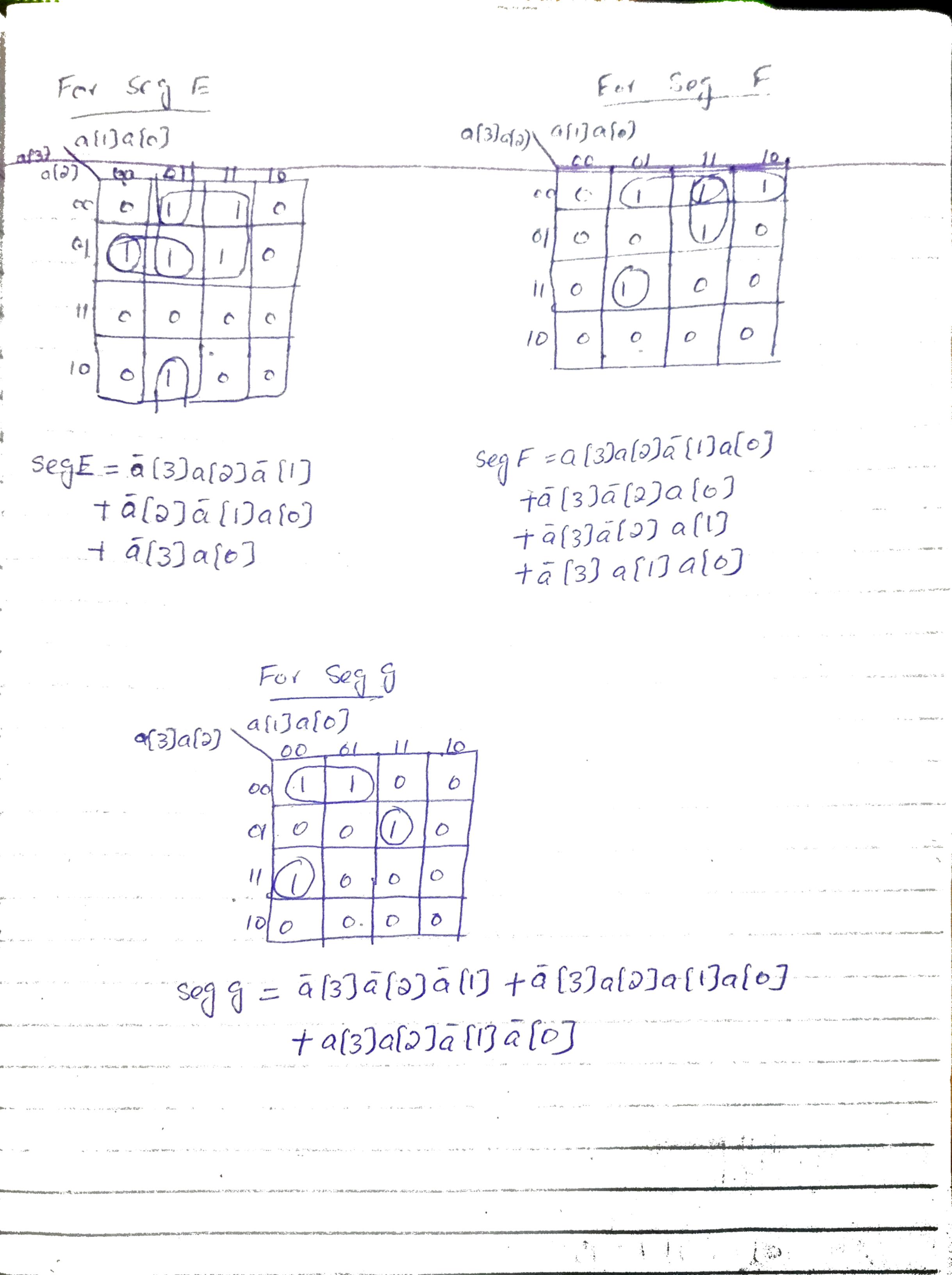
**(a)**

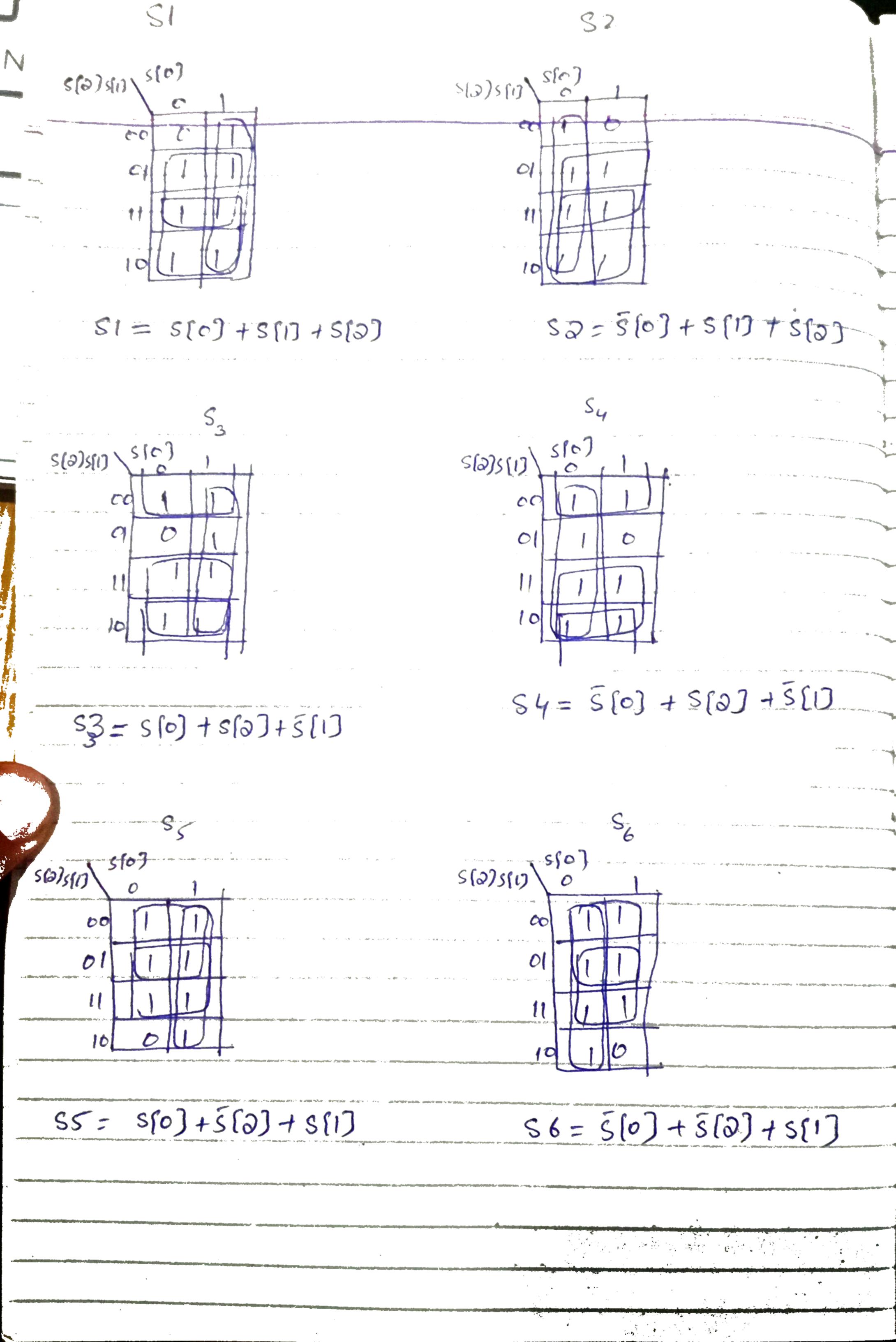


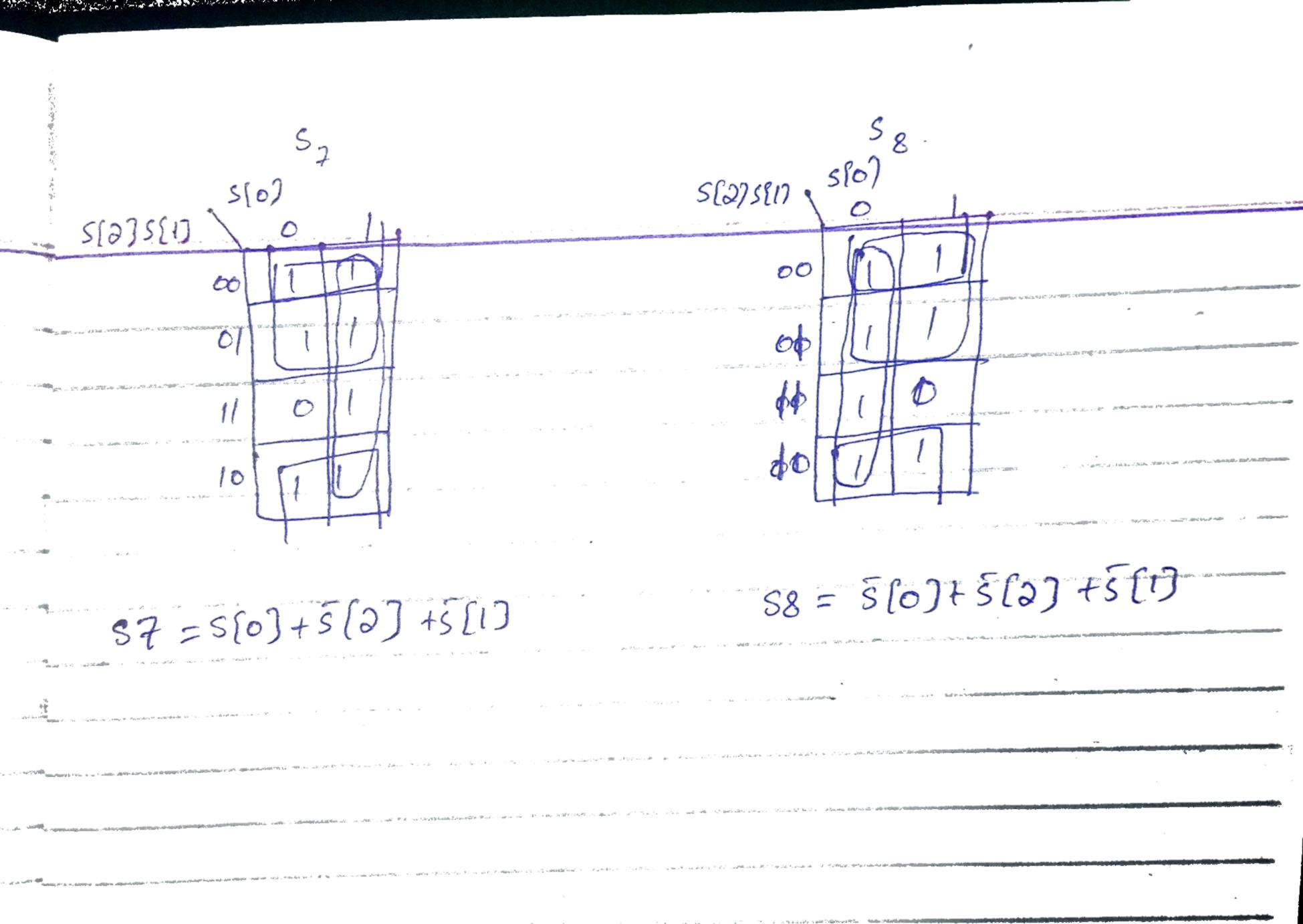


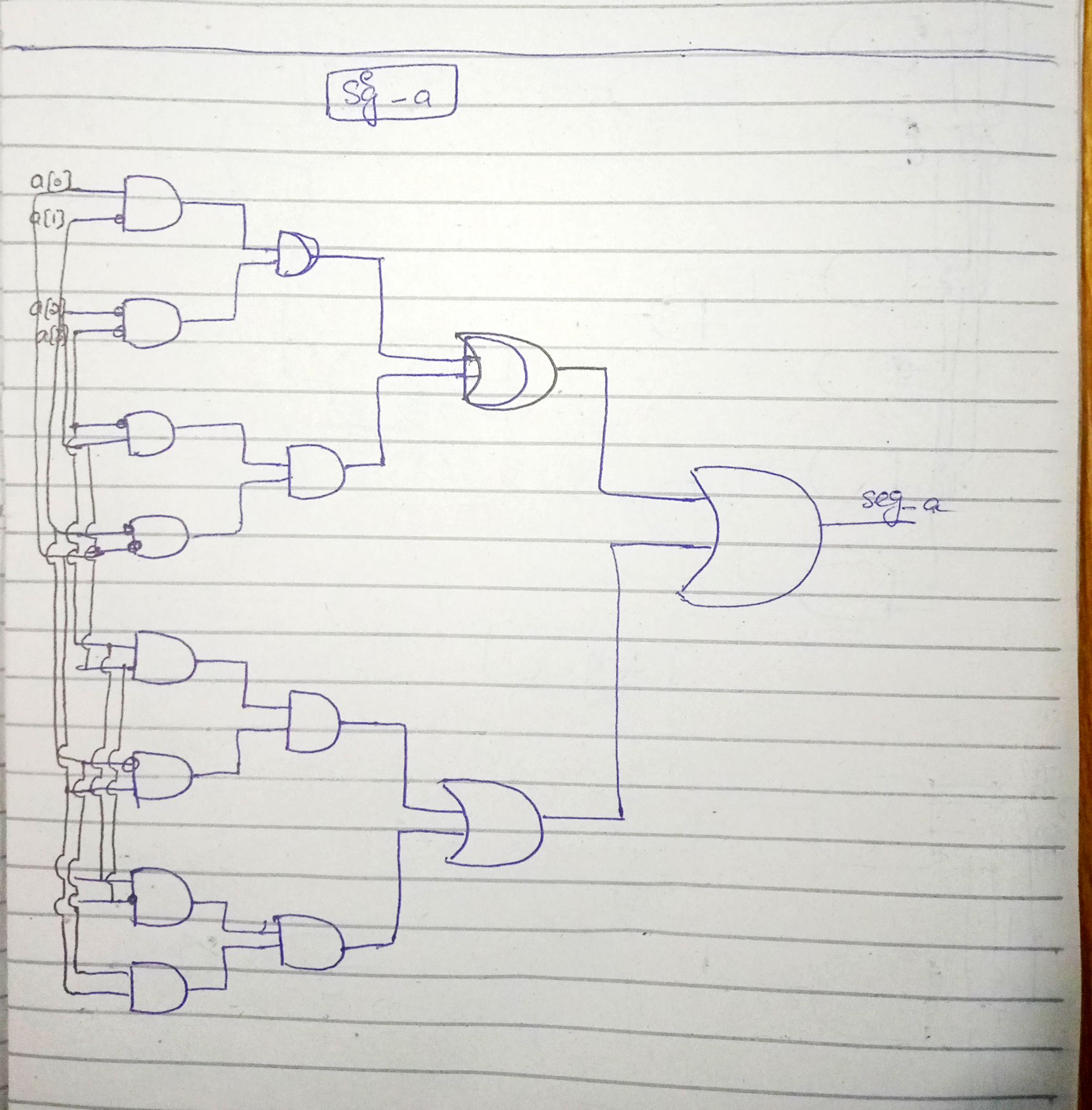
**(b) K-Maps**

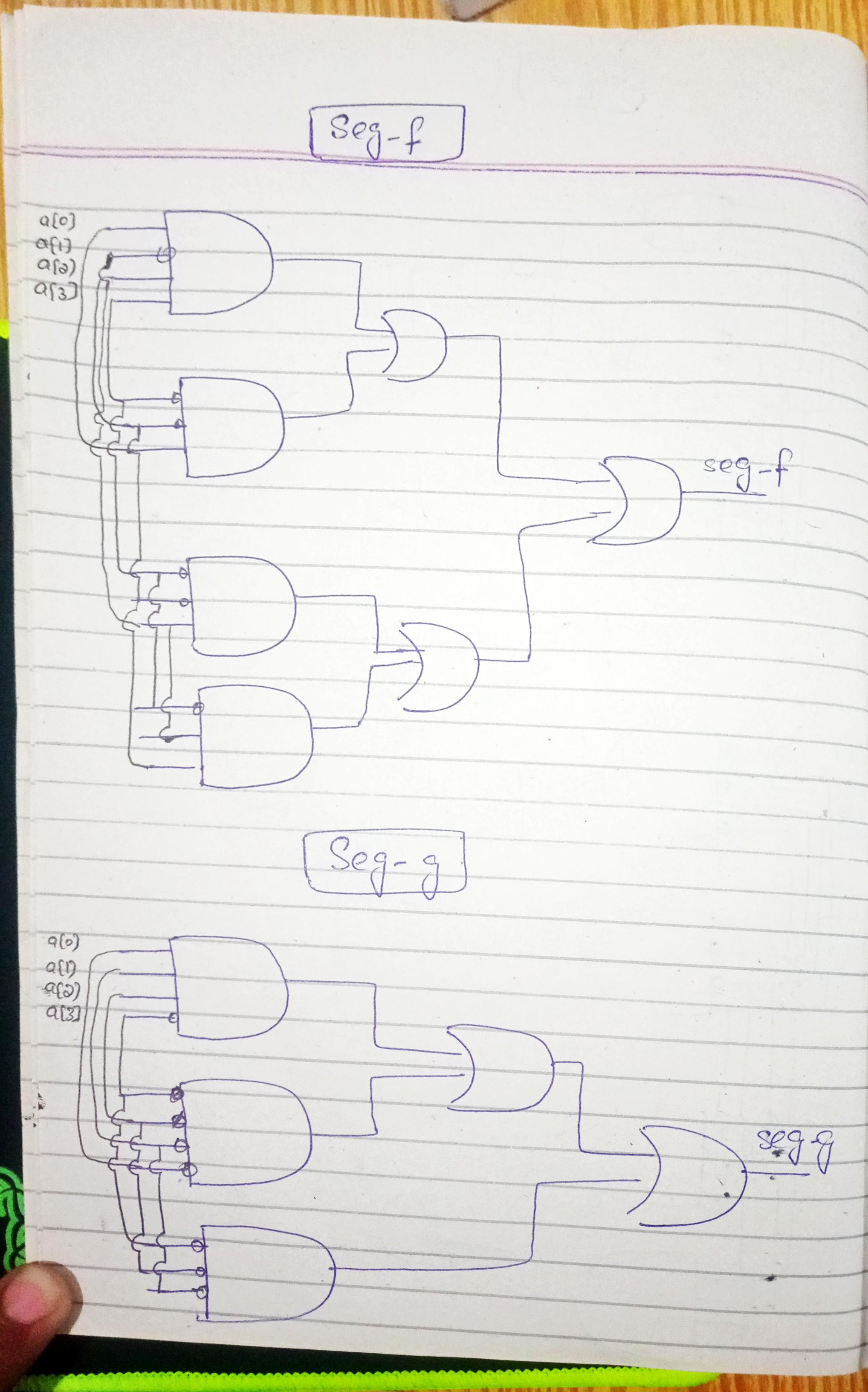
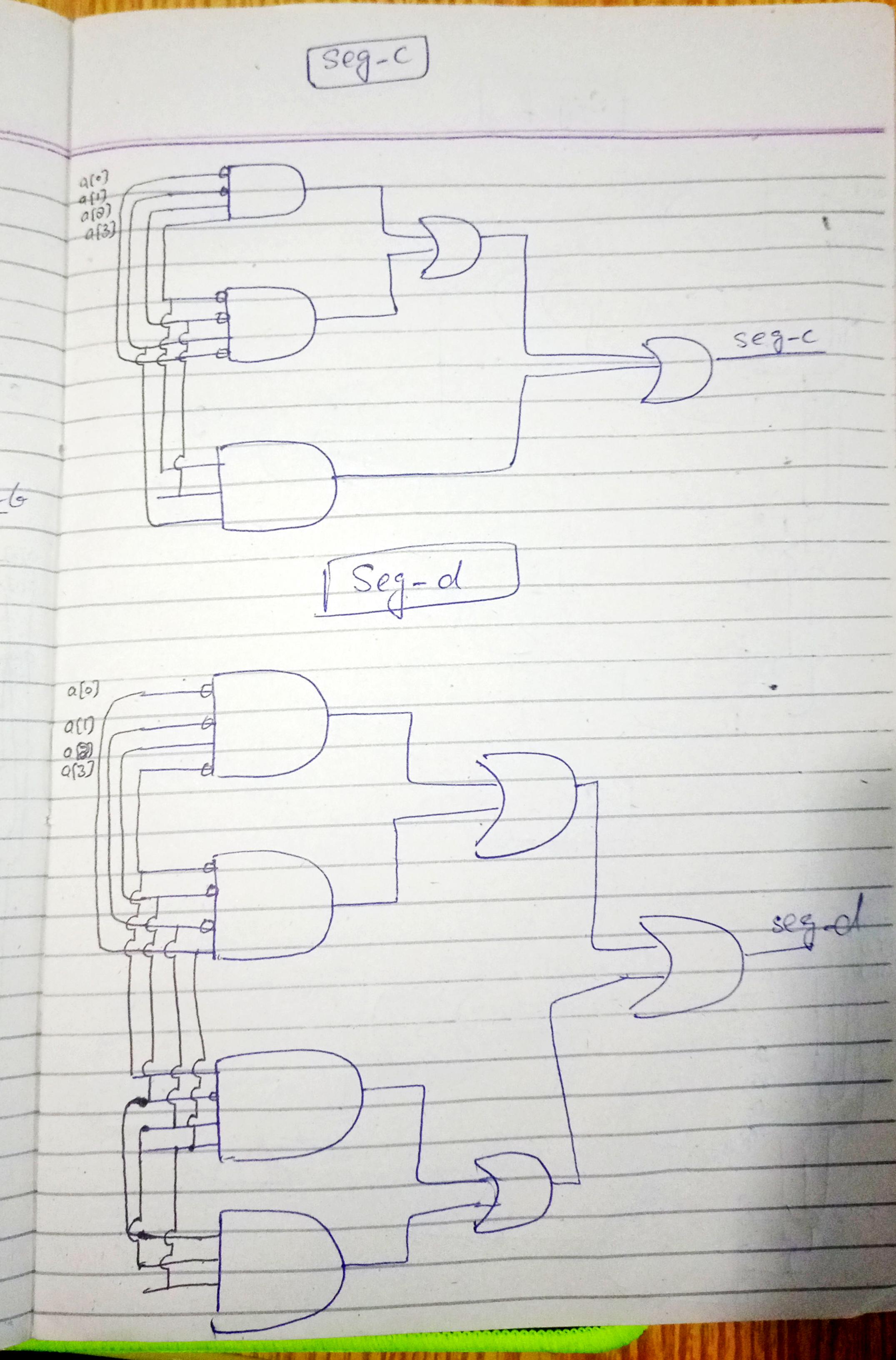
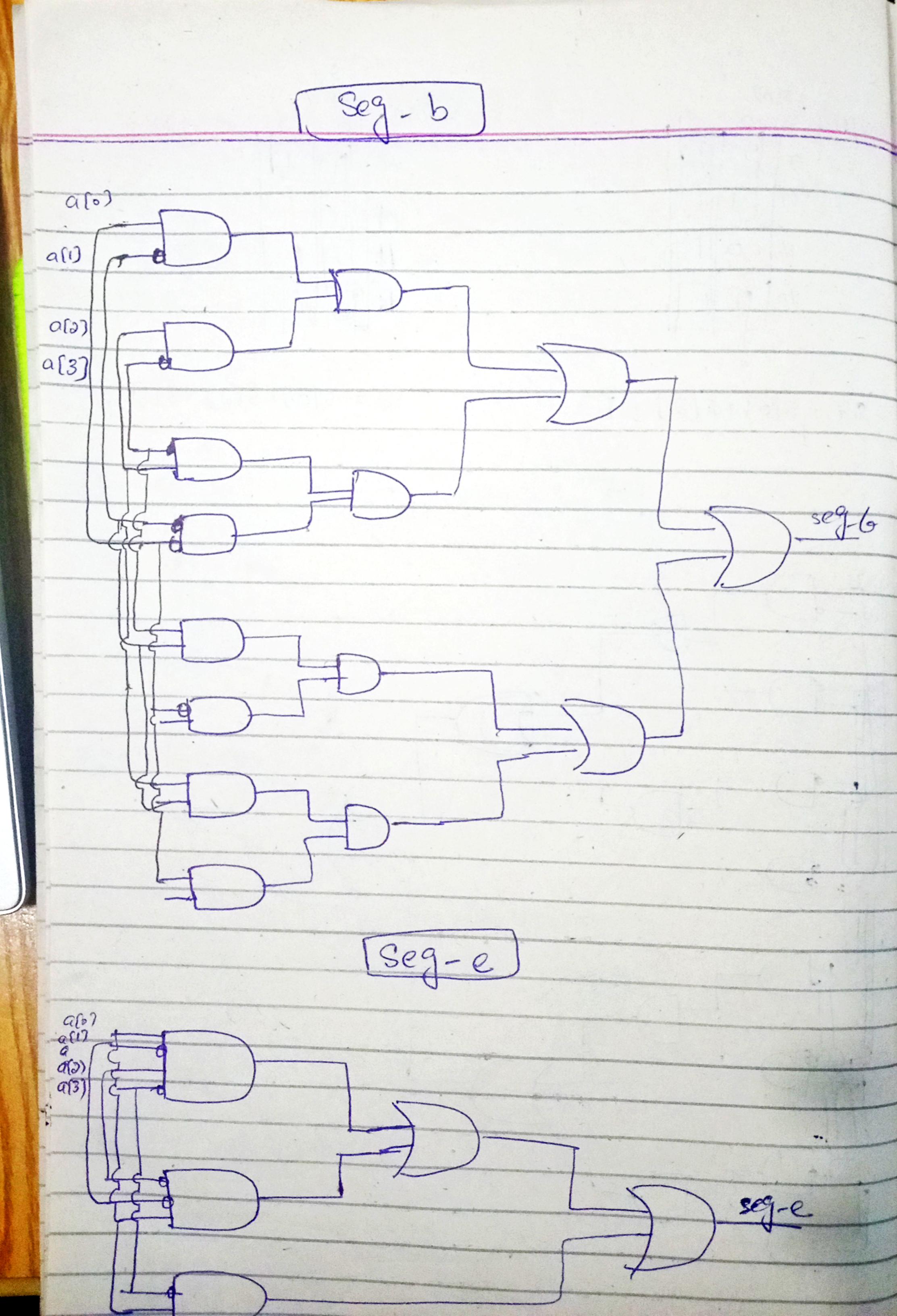




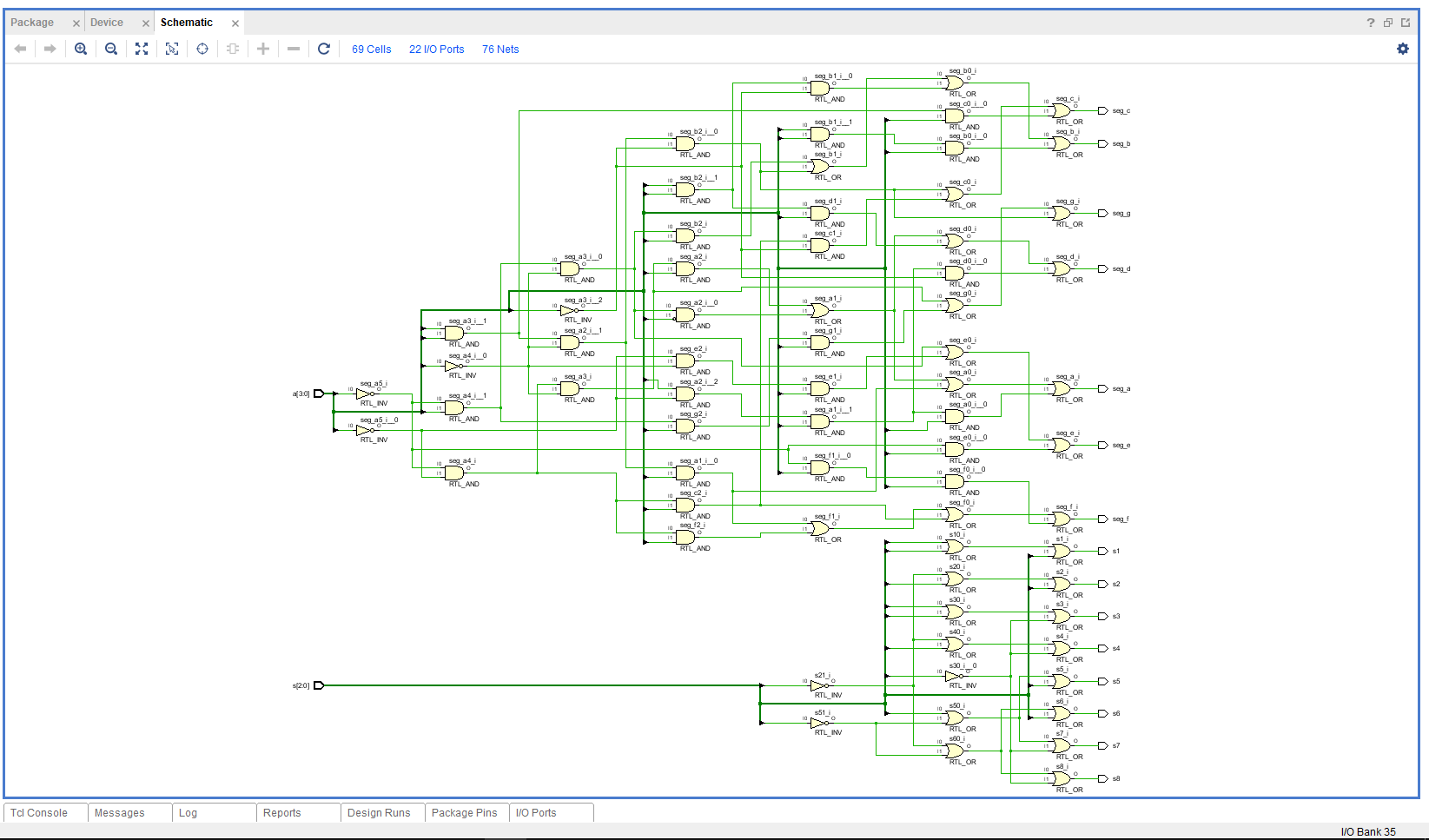




**(c)** 



**(d)**



**(e)**

Max. Combinational delay on Synthesis

From s [1] to s3 = 6.825

**(f)**

Max. Combinational delay on Implementation

From s [0] to s7 = 11.154

**(g) Resource Utilization**

|  |  |
| --- | --- |
| OBUF | 15 |
| LUT3 | 8 |
| LUT4 | 7 |
| IBUF | 7 |
| LUT AS LOGIC | 8 |